



1. Description

1.1. Project

Project Name	CDx_F150
Board Name	custom
Generated with:	STM32CubeMX 6.6.1
Date	10/05/2022

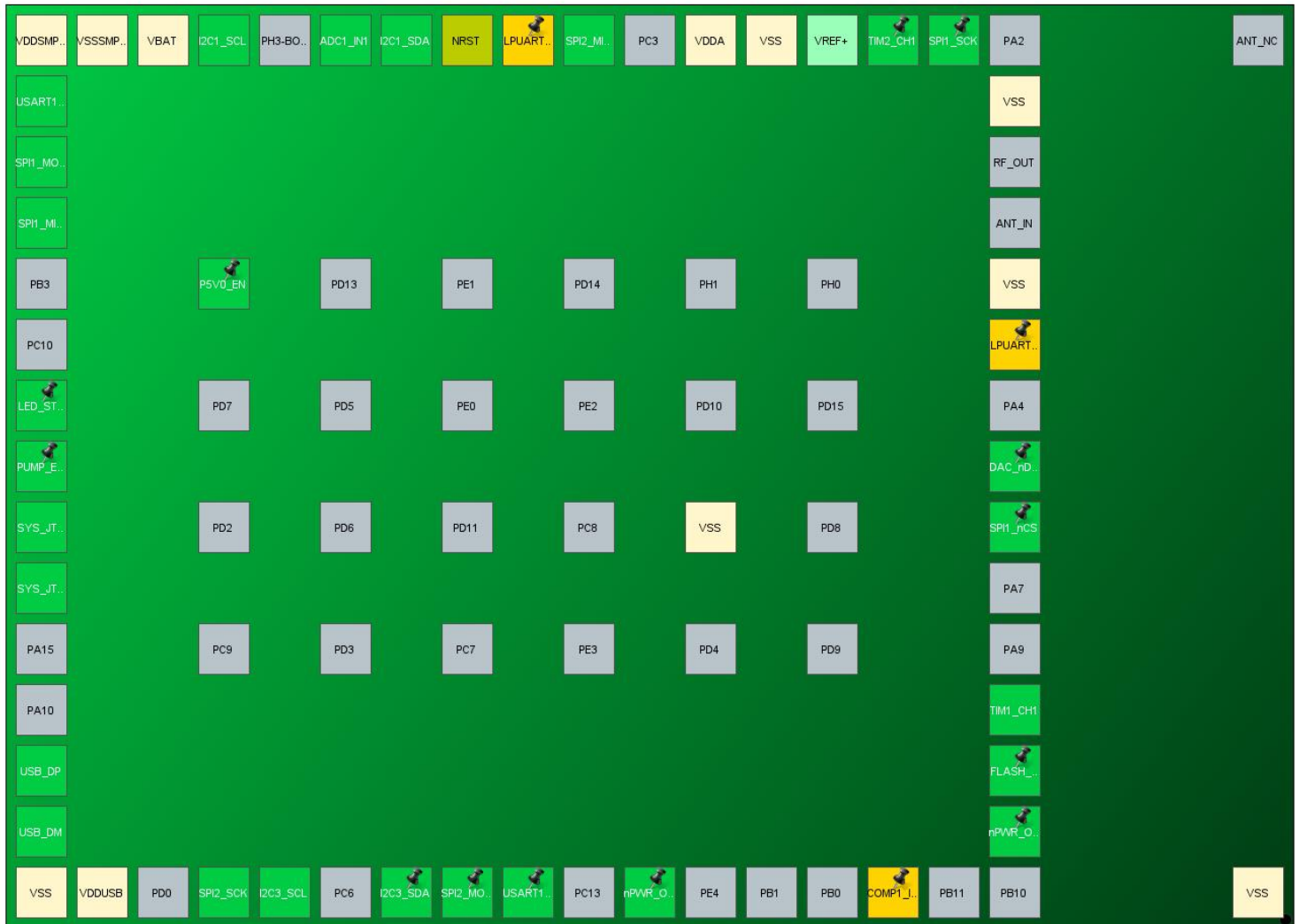
1.2. MCU

MCU Series	STM32WB
MCU Line	STM32WBxM Modules
MCU name	STM32WB5MMGHx
MCU Package	LGA86
MCU Pin number	86

1.3. Core(s) information

Core(s)	ARM Cortex-M4
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2. Pinout Configuration



LGA86 (Bottom view - Rotated +90°)

3. Pins Configuration

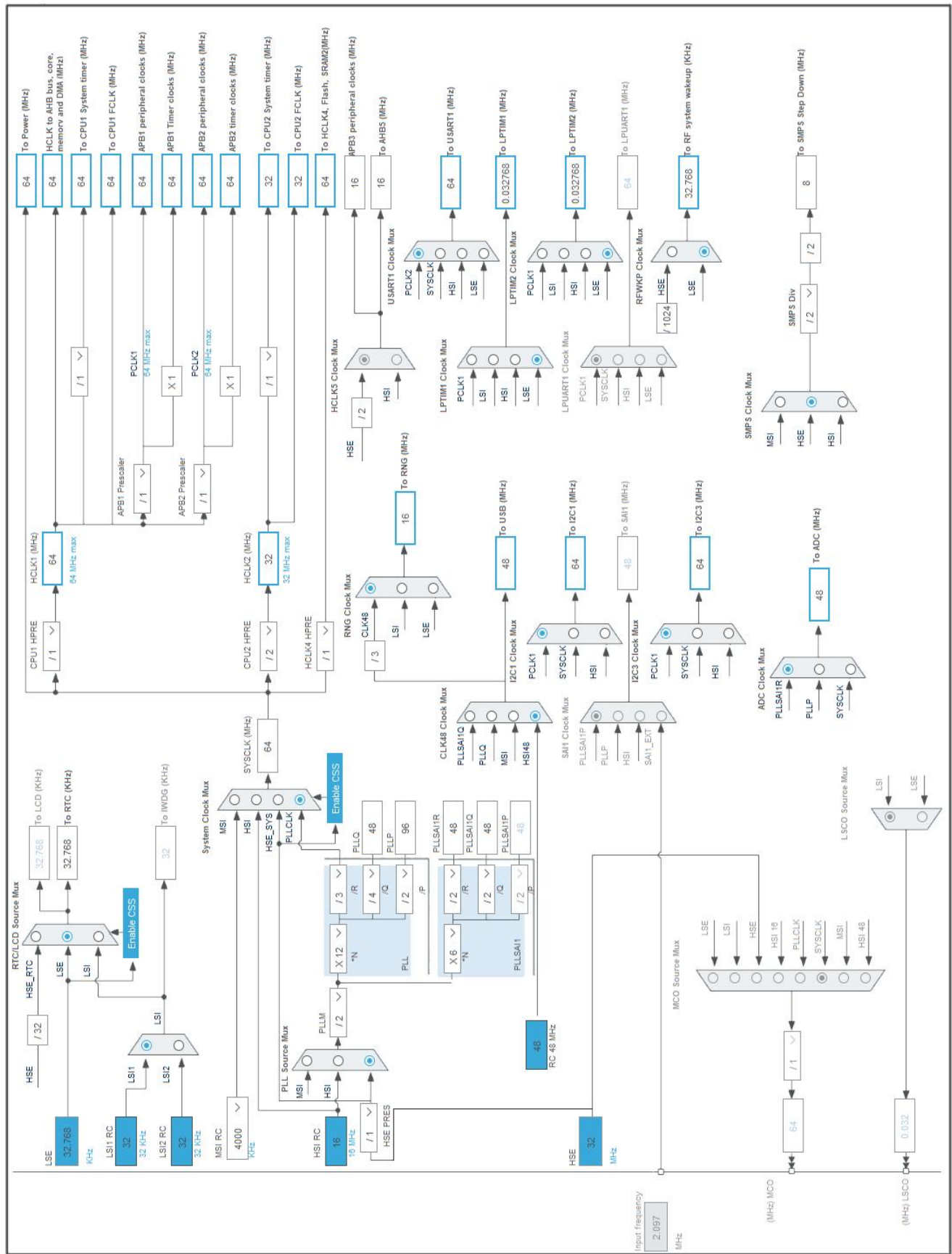
Pin Number LGA86	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
2	PA1	I/O	SPI1_SCK	
3	PA0	I/O	TIM2_CH1	
5	VSS	Power		
6	VDDA	Power		
8	PC2	I/O	SPI2_MISO	
9	PC1 *	I/O	LPUART1_TX	
10	NRST	Reset		
11	PB9	I/O	I2C1_SDA	
12	PC0	I/O	ADC1_IN1	
14	PB8	I/O	I2C1_SCL	
15	VBAT	Power		
16	VSSSMPS	Power		
17	VDDSMPS	Power		
18	PB7	I/O	USART1_RX	
19	PB5	I/O	SPI1_MOSI	
20	PB4	I/O	SPI1_MISO	
23	PC11 **	I/O	GPIO_Output	LED_STAT_EN
24	PC12 **	I/O	GPIO_Output	PUMP_ENn
25	PA13	I/O	SYS_JTMS-SWDIO	
26	PA14	I/O	SYS_JTCK-SWCLK	
29	PA12	I/O	USB_DP	
30	PA11	I/O	USB_DM	
31	VSS	Power		
32	VDDUSB	Power		
34	PD1	I/O	SPI2_SCK	
35	PB13	I/O	I2C3_SCL	
37	PB14	I/O	I2C3_SDA	
38	PB15	I/O	SPI2_MOSI	
39	PB6	I/O	USART1_TX	
41	PB12 **	I/O	GPIO_Output	nPWR_ON
45	PC5 *	I/O	COMP1_INP	
48	PB2 **	I/O	GPIO_Output	nPWR_OFF
49	PC4 **	I/O	GPIO_Output	FLASH_SPI2_nSS
50	PA8	I/O	TIM1_CH1	
53	PA6 **	I/O	GPIO_Output	SPI1_nCS
54	PA5 **	I/O	GPIO_Output	DAC_nDAC

Pin Number LGA86	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
56	PA3 *	I/O	LPUART1_RX	
57	VSS	Power		
60	VSS	Power		
66	PD12 **	I/O	GPIO_Output	P5V0_EN
84	VSS	Power		
86	VSS	Power		

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	CDx_F150
Project Folder	C:\Caire\F150\F150_MASTER
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_WB V1.14.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	Yes

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_CRC_Init	CRC
5	MX_RTC_Init	RTC
6	MX_ADC1_Init	ADC1
7	MX_I2C1_Init	I2C1
8	MX_I2C3_Init	I2C3
9	MX_RF_Init	RF
10	MX_SPI1_Init	SPI1
11	MX_TIM1_Init	TIM1

Rank	Function Name	Peripheral Instance Name
12	MX_TIM2_Init	TIM2
13	MX_TIM16_Init	TIM16
14	MX_LPTIM1_Init	LPTIM1
15	MX_LPTIM2_Init	LPTIM2
16	MX_SPI2_Init	SPI2
17	MX_IPCC_Init	IPCC
18	MX_USB_Device_Init	USB_DEVICE
19	MX_AES1_Init	AES1
20	MX_PKA_Init	PKA
21	MX_RNG_Init	RNG
22	APPE_Init	STM32_WPAN
23	MX_USART1_UART_Init	USART1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32WB
Line	STM32WBxM Modules
MCU	STM32WB5MMGHx
Datasheet	DS13252_Rev3

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

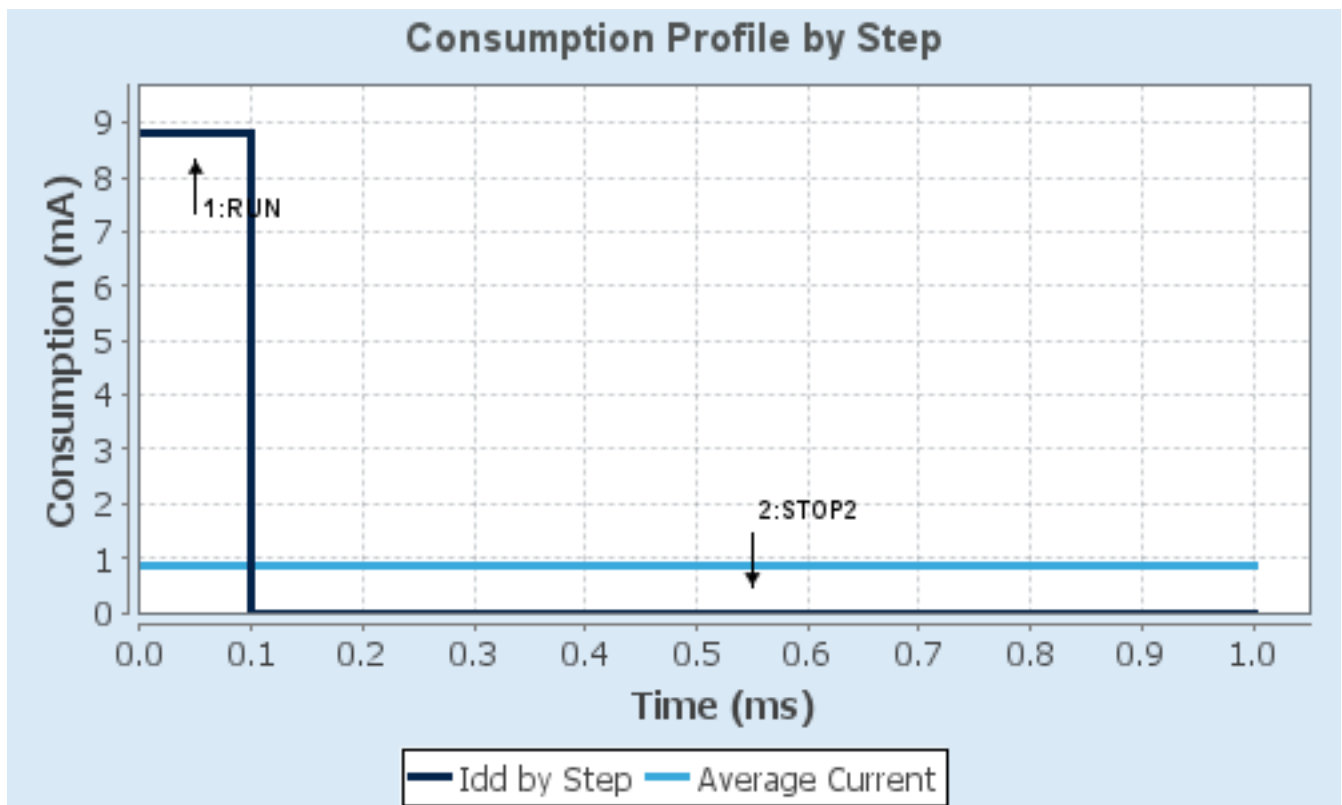
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM1/Flash-PowerDown	FLASH/ART/CACHE
CPU Frequency	64 MHz	0 Hz
Clock Configuration	HSI PLL Regulator_ON	ALL CLOCKS OFF Regulator ON
Clock Source Frequency	16 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	8.8 mA	1.85 μ A
Duration	0.1 ms	0.9 ms
DMIPS	80.0	0.0
Ta Max	104	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	881.66 μ A
Battery Life	5 months, 7 days, 21 hours	Average DMIPS	8.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

IN1: IN1 Single-ended

7.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten *
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Disable *
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ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable
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7.2. AES1

mode: Activated

7.2.1. Parameter Settings:

Algorithm:

Data encryption type	AES ECB
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Parameters:

Data type	32b(no swapping)
KeySize	128b
Encryption/Decryption key	00000000 00000000 00000000 00000000
Data width unit	Word
Key and IV configuration skip	Always

7.3. CRC

mode: Activated

7.3.1. Parameter Settings:

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

7.4. HSEM

mode: Activated

7.5. I2C1

I2C: I2C

7.5.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.6. I2C3

I2C: I2C

7.6.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.7. IPCC

mode: Activated

7.8. LPTIM1

Mode: Counts internal clock events

7.8.1. Parameter Settings:

Clock:

Clock Prescaler	Prescaler Div1
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Preload:

Update Mode	Update End Of Period *
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Trigger:

Trigger Source	Software Trigger
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7.9. LPTIM2

Mode: Counts internal clock events

7.9.1. Parameter Settings:

7.12. RF

mode: Activate RF

7.13. RNG

mode: Activated

7.13.1. Parameter Settings:

Clock Error Detection	Enable
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7.14. RTC

mode: Activate Clock Source

mode: Activate Calendar

7.14.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	CFG_RTC_ASYNC_PRESCALER
Synchronous Predivider value	CFG_RTC_SYNC_PRESCALER

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

7.15. SPI1

Mode: Full-Duplex Master

7.15.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits *
First Bit	MSB First
Clock Parameters:	
Prescaler (for Baud Rate)	2
Baud Rate	32.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge
Advanced Parameters:	
CRC Calculation	Disabled
NSSP Mode	Disabled *
NSS Signal Type	Software

7.16. SPI2

Mode: Full-Duplex Master

7.16.1. Parameter Settings:

Basic Parameters:	
Frame Format	Motorola
Data Size	8 Bits *
First Bit	MSB First
Clock Parameters:	
Prescaler (for Baud Rate)	2
Baud Rate	32.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge
Advanced Parameters:	
CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.17. SYS

Debug: Serial Wire

Timebase Source: TIM17

7.18. TIM1

Trigger Source: ITR0

Channel1: PWM Generation CH1

7.18.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	63 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	39 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable
Slave Mode Controller	Slave mode disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable
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PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	19 *
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.19. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.19.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	6399 *
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable
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PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.20. TIM16

mode: Activated

7.20.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	
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	6399 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	99 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Enable *

7.21. TINY_LPM

mode: Enabled

7.22. USART1

Mode: Asynchronous

7.22.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	8 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.23. USB

mode: Device (FS)

7.23.1. Parameter Settings:

Basic Parameters:

Speed	Full Speed 12MBit/s
Physical interface	Internal Phy
Sof Enable	Disabled

Power Parameters:

Low Power	Disabled
Link Power Management	Disabled
Battery Charging	Disabled

7.24. FREERTOS

Interface: CMSIS_V2

7.24.1. Config parameters:

API:

FreeRTOS API	CMSIS v2
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Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Enabled *

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled

QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled
OVERRIDE_DEFAULT_TICK_CONFIGURATION	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	0x8000 *
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Enabled *
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Enabled *
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Option2 *

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

CMSIS-RTOS V2 flags:

USE_OS2_THREAD_SUSPEND_RESUME	Enabled
USE_OS2_THREAD_ENUMERATE	Enabled
USE_OS2_EVENTFLAGS_FROM_ISR	Enabled
USE_OS2_THREAD_FLAGS	Enabled

USE_OS2_TIMER	Enabled
USE_OS2_MUTEX	Enabled

7.24.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Enabled *
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Enabled *
uxTaskGetStackHighWaterMark2	Disabled

7.24.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Enabled *
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Project settings (see parameter description first):

Use FW pack heap file	Enabled
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7.25. STM32_WPAN

mode: BLE

7.25.1. BLE Applications and Services:

BLE Wireless Stack:

BLE Wireless Stack Full

BLE Application Type:

BLE Application Type Server profile

Server Mode:

BT SIG Heart Rate Sensor **Disabled ***

BLE Services Configuration:

The device needs to support the Peripheral Role 1

The device needs to support the Central Role 0

BLE_CFG_SVC_MAX_NBR_CB 7

BLE_CFG_CLT_MAX_NBR_CB **5 ***

7.25.2. Configuration:

HW Timer Server:

CFG_HW_TS_MAX_NBR_CONCURRENT_TIMER 6

CFG_HW_TS_NVIC_RTC_WAKEUP_IT_PREEMPTPRIO 3

CFG_HW_TS_NVIC_RTC_WAKEUP_IT_SUBPRIO 0

CFG_HW_TS_USE_PRIMASK_AS_CRITICAL_SECTION 1

CFG_HW_TS_RTC_HANDLER_MAX_DELAY (10 * (LSI_VALUE/1000))

CFG_HW_TS_RTC_WAKEUP_HANDLER_ID RTC_WKUP_IRQn

HW UART:

CFG_HW_LPUART1_ENABLED Disabled

CFG_HW_LPUART1_DMA_TX_SUPPORTED Disabled

CFG_HW_USART1_ENABLED **Enabled ***

CFG_HW_USART1_DMA_TX_SUPPORTED Disabled

Generic parameters:

CFG_HW_RESET_BY_FW Enabled

CFG_USE_SMPS Disabled

CFG_LPM_SUPPORTED **Enabled ***

CFG_DEBUGGER_SUPPORTED Enabled

CFG_DEBUG_BLE_TRACE **Enabled ***

CFG_DEBUG_APP_TRACE **Enabled ***

CFG_DEBUG_TRACE_LIGHT Disabled

CFG_DEBUG_TRACE_FULL **Enabled ***

DBG_TRACE_USE_CIRCULAR_QUEUE Enabled

DBG_TRACE_MSG_QUEUE_SIZE 4096

MAX_DBG_TRACE_MSG_SIZE 1024

Application parameters:

CFG_TX_POWER	-0.15dBm (0x18)
CFG_DEBUG_TRACE_UART	hw_uart1 *
CFG_CONSOLE_MENU	No UART selected. You need to activate LPUART1 (if available)
CFG_ADV_BD_ADDRESS	0x000000000000 *
CFG_FAST_CONN_ADV_INTERVAL_MIN	80
CFG_FAST_CONN_ADV_INTERVAL_MAX	100
CFG_LP_CONN_ADV_INTERVAL_MIN	1000
CFG_LP_CONN_ADV_INTERVAL_MAX	2500
CFG_IO_CAPABILITY	Display only (0x00) *
CFG_MITM_PROTECTION	MITM protection required (0x01)
CFG_RTCCLK_DIVIDER_CONF	0
CFG_RTCCLK_DIV	16
CFG_RTC_WUCKSEL_DIVIDER	0
CFG_RTC_ASYNC_PRESCALER	0x0F *
CFG_RTC_SYNC_PRESCALER	0x7FFF *
CFG_BLE_NUM_LINK	2
CFG_BLE_NUM_GATT_SERVICES	8
CFG_BLE_NUM_GATT_ATTRIBUTES	68
CFG_BLE_MAX_ATT_MTU	156
CFG_BLE_ATT_VALUE_ARRAY_SIZE	1344
CFG_BLE_DATA_LENGTH_EXTENSION	Enabled
CFG_BLE_SLAVE_SCA	500
CFG_BLE_MASTER_SCA	0
CFG_BLE_HSE_STARTUP_TIME	0x148 *
CFG_BLE_MAX_CONN_EVENT_LENGTH	0xFFFFFFFF *
CFG_BLE_VITERBI_MODE	Enabled
CFG_BLE_OPTIONS	BLE stack Options flags:
- CFG_BLE_OPTIONS_LL	SHCI_C2_BLE_INIT_OPTIONS_LL_HOST
- CFG_BLE_OPTIONS_SVC	SHCI_C2_BLE_INIT_OPTIONS_WITH_SVC_CHANGE_DESC
- CFG_BLE_OPTIONS_DEVICE_NAME	SHCI_C2_BLE_INIT_OPTIONS_DEVICE_NAME_RW
- CFG_BLE_OPTIONS_EXT_ADV	SHCI_C2_BLE_INIT_OPTIONS_NO_EXT_ADV
- CFG_BLE_OPTIONS_CS_ALGO	SHCI_C2_BLE_INIT_OPTIONS_NO_CS_ALGO2
- CFG_BLE_OPTIONS_POWER_CLASS	SHCI_C2_BLE_INIT_OPTIONS_POWER_CLASS_2_3
CFG_BLE_MAX_COC_INITIATOR_NBR	32
CFG_BLE_MIN_TX_POWER	0

CFG_BLE_MAX_TX_POWER	0
CFG_BLE_RX_MODEL_CONFIG	SHCI_C2_BLE_INIT_RX_MODEL_AGC _RSSI_LEGACY
CFG_BLE_MAX_ADV_SET_NBR	3
CFG_BLE_MAX_ADV_DATA_LEN	1650
CFG_BLE_TX_PATH_COMPENS	0
CFG_BLE_RX_PATH_COMPENS	0
CFG_TLBLE_EVT_QUEUE_LENGTH	5
CFG_TLBLE_MOST_EVENT_PAYLOAD_SIZE	255
Pairing parameters:	
CFG_BONDING_MODE	Bonding mode(0x01) *
CFG_USED_FIXED_PIN	Use a fixed pin (0x00)
CFG_FIXED_PIN	123456 *
CFG_ENCRYPTION_KEY_SIZE_MAX	16
CFG_ENCRYPTION_KEY_SIZE_MIN	8
CFG_SC_SUPPORT	Secure Connections Paring supported and mandatory(0x02) *
CFG_BLE_IRK	12, 34, 56, 78, 9A, BC, DE, F0, 12, 34, 56, 78, 9A, BC, DE, F0
CFG_BLE_ERK	FE, DC, BA, 09, 87, 65, 43, 21, FE, DC, BA, 09, 87, 65, 43, 21
CFG_KEYPRESS_NOTIFICATION_SUPPORT	Keypress notification not supported (0x00)
Debug options:	
BLE_DBG_APP_EN	Enabled *

7.26. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

7.26.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

Class Parameters:

USB CDC Rx Buffer Size	2048
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USB CDC Tx Buffer Size

2048

7.26.2. Device Descriptor:

Device Descriptor:

VID (Vendor Identifier)

1155

LANGID_STRING (Language Identifier)

English(United States)

MANUFACTURER_STRING (Manufacturer Identifier)

STMicroelectronics

Device Descriptor FS:

PID (Product Identifier)

22336

PRODUCT_STRING (Product Identifier)

STM32 Virtual ComPort

CONFIGURATION_STRING (Configuration Identifier)

CDC Config

INTERFACE_STRING (Interface Identifier)

CDC Interface

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up *	Low	
	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up *	Low	
I2C3	PB13	I2C3_SCL	Alternate Function Open Drain	Pull-up *	Low	
	PB14	I2C3_SDA	Alternate Function Open Drain	Pull-up *	Low	
SPI1	PA1	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI2	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PD1	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	High *	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB	PA12	USB_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA11	USB_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
Single Mapped Signals	PC1	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	COMP1_INP	Analog mode	No pull-up and no pull-down	n/a	
	PA3	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_STAT_EN
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PUMP_ENn
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	nPWR_ON
	PB2	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	nPWR_OFF
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FLASH_SPI2_nSS
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_nCS
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DAC_nDAC
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	P5V0_EN

8.2. DMA configuration

DMA request	Stream	Direction	Priority
I2C1_RX	DMA1_Channel3	Peripheral To Memory	Low
I2C1_TX	DMA1_Channel4	Memory To Peripheral	Low
ADC1	DMA1_Channel5	Peripheral To Memory	Low
AES1_IN	DMA1_Channel2	Memory To Peripheral	Low
AES1_OUT	DMA1_Channel1	Peripheral To Memory	Low

I2C1_RX: DMA1_Channel3 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

I2C1_TX: DMA1_Channel4 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

ADC1: DMA1_Channel5 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Half Word
Memory Data Width: Half Word

AES1_IN: DMA1_Channel2 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte

Memory Data Width: Byte

AES1_OUT: DMA1_Channel1 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
RCC global interrupt	true	10	0
DMA1 channel1 global interrupt	true	10	0
DMA1 channel2 global interrupt	true	10	0
DMA1 channel3 global interrupt	true	10	0
DMA1 channel4 global interrupt	true	10	0
DMA1 channel5 global interrupt	true	10	0
USB low priority interrupt, USB wake-up interrupt through EXTI line 28	true	5	0
TIM1 update interrupt and TIM16 global interrupt	true	10	0
TIM1 trigger and commutation interrupts and TIM17 global interrupt	true	15	0
TIM2 global interrupt	true	10	0
I2C1 event interrupt	true	10	0
I2C1 error interrupt	true	10	0
I2C3 event interrupt	true	10	0
I2C3 error interrupt	true	10	0
USART1 global interrupt	true	10	0
IPCC RX occupied interrupt	true	6	0
IPCC TX free interrupt	true	6	0
HSEM global interrupt	true	6	0
LPTIM1 global interrupt	true	10	0
LPTIM2 global interrupt	true	10	0
PVD/PVM0/PVM2 interrupts through EXTI lines 16/31/33	unused		
Flash global interrupt	unused		
ADC1 global interrupt	unused		
USB high priority interrupt	unused		
CPU2 SEV interrupt through EXTI line 40 and PWR CPU2 HOLD wake-up interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM1 break interrupt		unused	
TIM1 capture compare interrupt		unused	
PKA interrupt		unused	
SPI1 global interrupt		unused	
SPI2 global interrupt		unused	
PWR switching on the fly, end of BLE activity, end of 802.15.4 activity, end of critical radio phase interrupt		unused	
AES1 global interrupt		unused	
RNG global interrupt		unused	
FPU global interrupt		unused	

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
RCC global interrupt	false	true	false
DMA1 channel1 global interrupt	false	true	true
DMA1 channel2 global interrupt	false	true	true
DMA1 channel3 global interrupt	false	true	true
DMA1 channel4 global interrupt	false	true	true
DMA1 channel5 global interrupt	false	true	true
USB low priority interrupt, USB wake-up interrupt through EXTI line 28	false	true	true
TIM1 update interrupt and TIM16 global interrupt	false	true	true
TIM1 trigger and commutation interrupts and TIM17 global interrupt	false	true	true
TIM2 global interrupt	false	true	true
I2C1 event interrupt	false	true	true
I2C1 error interrupt	false	true	true
I2C3 event interrupt	false	true	true
I2C3 error interrupt	false	true	true
USART1 global interrupt	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
IPCC RX occupied interrupt	false	true	true
IPCC TX free interrupt	false	true	true
HSEM global interrupt	false	true	true
LPTIM1 global interrupt	false	true	true
LPTIM2 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type	Link
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